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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,083	10/27/2003	Akira Tomono	03180.0340	8467

7590 12/28/2004

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,083	TOMONO ET AL.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *7-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/693083 Attorney's Docket #: 03180.0340-00
Filing Date: 10/27/2003; claimed foreign priority to 6/16/2003

Applicant: Tomono et al.

Examiner: Alexander Williams

Applicant's election of species corresponding to figure 1 (claims 1 to 6), filed 9/30/2004, has been acknowledged.

This application contains claims 7 to 15 drawn to an invention non-elected without traverse.

This application contains claims 16 to 22 drawn to an invention non-elected without traverse.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The disclosure is objected to because of the following informalities: On page 9, lines 5 and 6, "alminium" should be –aluminum--.

Appropriate correction is required.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claims 2 and 3 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, it is unclear and confusing to what is meant by "wherein the second solder balls include at least one material selected from the group consisting of Sn-Ag, An-Ag-Cu, Sn-Pb, and Sn-Zn." Does this mean that one of the material in the composition claimed can be used?

In claim 3, it is unclear and confusing to what is meant by "wherein the second solde balls includes **at least one material** selected from the group consisting of Sn-Ag, An-Ag-Cu, Sn-Pb, and Sn-Zn." Does this mean that one of the material in the composition claimed can be used?

In claim 3, it is unclear and confusing to what is meant by "**An**-Ag-Cu." What does the "An" represent in the composition?

Any of claims 2 and 3 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 6, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Iijima (U.S Patent Application Publication # 2004/0155358 A1).

1. Iijima (figures 1 to 12C) specifically figure 7C show a packaging assembly comprising: a substrate **1** defined by a first surface and a second surface opposing to the first surface; a plurality of chip-site lands **6a-d** disposed on the first surface; a plurality of first solder balls **18a-d** connected to the chip-site lands; a plurality of second solder balls **17a-d** connected to the first solder balls including solder materials having higher melting temperatures than the first solder balls; a semiconductor chip **7** having a plurality of bonding pads **4a-d** connected to the second solder balls on a surface of the semiconductor chip; and an underfill resin **8** disposed around the first and second solder balls.

2. The packaging assembly of claim 1, Iijima show wherein the first solder balls **18a-d** include at least one material selected from the group consisting of Sn-Bi, **Sn-Bi-Ag**, Sn-Zn, Sn-Zn-Bi, Sn-Bi-In, Bi-In, Sn-In, Bi-Pd, In-Ag, and Sn-Pb.

3. The packaging assembly of claim 1, Iijima show wherein the second solder balls include at least one material selected from the group consisting of Sn-Ag, An-Ag-Cu, Sn-Pb, and Sn-Zn.

4. The packaging assembly of claim 1, Iijima show wherein a protective film containing an organic synthetic resin is disposed on the surface of the semiconductor chip.
5. The packaging assembly of claim 1, Iijima show wherein a low dielectric constant film **11** is stacked on the surface of the semiconductor chip.
6. The packaging assembly of claim 5, Iijima show wherein an effective dielectric constant of the low dielectric constant film is equal to or less than 3.5 (inherit since the it is a low dielectric material).

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Claims 1 to 6, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Soga et al. (U.S. Patent Application Publication # 2004/0007384 A1).
1. Soga et al. (figures 1 to 21b) specifically figure 16 show a packaging assembly comprising: a substrate **14** defined by a first surface and a second surface opposing to the first surface; a plurality of chip-site lands **82** disposed on the first surface; a plurality of first solder balls **85** connected to the chip-site lands; a plurality of second solder balls **80** connected to the first solder balls including solder materials having higher melting temperatures than the first solder balls; a semiconductor chip **25** having a plurality of bonding pads **82,83** connected to the second solder balls on a surface of the semiconductor chip; and an underfill resin **81** disposed around the first and second solder balls.
2. The packaging assembly of claim 1, Soga et al. show wherein the first solder balls include at least one material selected from the group consisting of Sn-Bi, Sn-Bi-Ag, Sn-Zn, Sn-Zn-Bi, Sn-Bi-In, Bi-In, Sn-In, Bi-Pd, In-Ag, and Sn-Pb.
3. The packaging assembly of claim 1, Soga et al. show wherein the second solder balls include at least one material selected from the group consisting of Sn-Ag, An-Ag-Cu, Sn-Pb, and Sn-Zn.
4. The packaging assembly of claim 1, Soga et al. show wherein a protective film containing an organic synthetic resin is disposed on the surface of the semiconductor chip.

5. The packaging assembly of claim 1, Soga et al. show wherein a low dielectric constant film **90** is stacked on the surface of the semiconductor chip (see figure 18a).
6. The packaging assembly of claim 5, Soga et al. show wherein an effective dielectric constant of the low dielectric constant film is equal to or less than 3.5.

Claims 1 to 6, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kaneshiro (Japan Patent # 5-74778) in view of Soga et al. (U.S. Patent Application Publication # 2004/0007384 A1).
1. Kaneshiro (figures 1 to 11) specifically figures 9 and 10 show a packaging assembly comprising: a substrate **1** defined by a first surface and a second surface opposing to the first surface; a plurality of chip-site lands **(inherit)** disposed on the first surface; a plurality of first solder balls **4** connected to the chip-site lands; a plurality of second solder balls **5** connected to the first solder balls including solder materials having higher melting temperatures than the first solder balls; a semiconductor chip having a plurality of bonding pads connected to the second solder balls on a surface of the semiconductor chip; but fail to explicitly show an underfill resin disposed around the first and second solder balls. However, it is well understood in the art to use underfill around solder ball.

Soga et al. is cited for showing a electronic device. Specifically, Soga et al. (figures 1 to 21b) specifically figure 16 discloses an underfill resin **81** disposed around the first and second solder balls **80,84** for the purpose of providing an electronic device which solder bonding portions capable of maintaining bonding strength at a high temperature.
2. The packaging assembly of claim 1, the combination with Kaneshiro show wherein the first solder balls **4** include at least one material selected from the group consisting of Sn-Bi, Sn-Bi-Ag, Sn-Zn, Sn-Zn-Bi, Sn-Bi-In, Bi-In, Sn-In, Bi-Pd, **In-Ag**, and Sn-Pb.
3. The packaging assembly of claim 1, the combination with Kaneshiro show wherein the second solder balls **5** include at least **one** material selected from the group consisting of Sn-**Ag**, An-Ag-**Cu**, Sn-Pb, and Sn-Zn.
4. The packaging assembly of claim 1, the combination with Soga et al. showing wherein a protective film containing an organic synthetic resin is disposed on the surface of the semiconductor chip.
5. The packaging assembly of claim 1, the combination with Soga et al. showing wherein a low dielectric constant film **90** is stacked on the surface of the semiconductor chip (see figure 18a).

6. The packaging assembly of claim 5, the combination with Soga et al. showing wherein an effective dielectric constant of the low dielectric constant film is equal to or less than 3.5 (inherit).

Therefore, it would have been obvious to one of ordinary skill in the art to use Soga et al.'s underfill to modify Kaneshiro's device for the purpose of providing an electronic device which solder bonding portions capable of maintaining bonding strength at a high temperature.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/772,778,779,780,737,738,734,741,686,685,723	12/21/04
Other Documentation: foreign patents and literature in 257/772,778,779,780,737,738,734,741,686,685,723	12/21/04
Electronic data base(s): U.S. Patents	12/21/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
12/21/04

Primary Patent Examiner
Alexander O. Williams